CIO-DIO24
CIO-DIO24H
CIO-DIO24/CTR3

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ComputerBoards, Inc.
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EC Declaration of Conformity

We, ComputerBoards, Inc., declare under sole responsibility that the product:

Part Number	Description
CIO-DIO24	Digital I/O board
CIO-DIO24H	Dig I/O brd w/High Current output
CIO-DIO24/CTR	Digital I/O board with counter

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

The trick to using a voltage divider is to choose two resistors with the proper proportions relative to the full scale of the digital input and the maximum signal voltage.

The phenomena of dropping the voltage proportionally is often called attenuation. The formula for attenuation is:

$$\text{Attenuation} = \frac{R1+R2}{R2}$$

The variable *Attenuation* is the proportional difference between the signal voltage max and the full scale of the analog input.

$$2 = \frac{10K+10K}{10K}$$

For example, if the signal varies between 0 and 10 volts and you wish to measure that with an CIO-DIO board with a full scale range of 0 to 5 volts, the *Attenuation* is 2:1 or just 2.

$$R1=(A-1)*R2$$

For a given attentuation, pick a handy resistor and call it R2, then use this formula to calculate R1.

Digital inputs can readily use voltage dividers. For example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to the CIO-DIO24 digital inputs. The voltage must be dropped to 5 volts max when on. The Attenuation is 24:5 or 4.8. Use the equation above to find an appropriate R1 if R2 is 1K. Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

IMPORTANT NOTE

The resistors, R1 and R2, are going to dissipate all the power in the divider circuit according to the equation Current = Voltage / Resistance. The higher the value of the resistance (R1 + R2) the less power dissipated by the divider circuit. Here is a simple rule:

For Attenuation of 5:1 or less, no resistor should be less than 10K.

For Attenuation of greater than 5:1, no resistor should be less than 1K.

The CIO-TERMINAL has the circuitry on board to create custom voltage dividers. The CIO-TERMINAL is a 16" by 4" screw terminal board with two 37 pin D type connectors and 56 screw terminals (12 - 22 AWG). Designed for table top, wall or rack mounting, the board provides prototype, divider circuit, filter circuit and pull-up resistor positions which you may complete with the proper value components for your application.

TABLE OF CONTENTS

INTRODUCTION

This manual provides information on the CIO-DIO24, CIO-DIO24H and CIO-DIO24/CTR3 digital I/O boards and accessories. The manual is organized into separate sections for those aspects of a product which are unique. Some issues, such as simple programming and electronic interfacing are applicable to all of the digital boards.

The CIO-DIO24 is a single 82C55 digital I/O chip interfaced to the PC bus, with all its I/O lines accessable through the board's 37 pin connector. The I/O pins of an 82C55 are CMOS TTL level.

CIO-DIO24H is a high drive, 24 line digital I/O board. The control register which sets the direction of the I/O ports is identical to an 82C55 in mode 0 (see 82C55 data sheet). The I/O pins are high drive TTL capable of sourcing 15mA and sinking 64mA.

CIO-DIO24/CTR3 is a CIO-DIO24 with an 82C54 counter added. The 82C54 is a 10MHz down-counter chip with three 16 bit counters. The functions of the counter (Input, Gate and Output) are brought out to those pins which are used for bus power access on the CIO-DIO24 and CIO-DIO24H. The CIO-DIO24/CTR3 uses 8 I/O addresses. The lower four are occupied by the 82C55 digital I/O chip and the upper four are occupied by the 82C54 counter timer chip.

All these boards have the same connector pin-out and respond to the same software instructions. Each board is explained in detail.

This manual provides information on programming the 82C55 in mode 0. Those wishing to use the 82C55 in modes 1 or 2, or who wish to program the 82C54 counter on the CIO-DIO24/CTR3, must procure a data book from Intel Corporation Literature Department.

All these products are supported by the Universal Library programming library. As an owner of this product, you are entitled to the latest revision of the manual and software. Just call with your current revision numbers handy, and request an update be sent to you.

TTL TO SOLID STATE RELAYS

Many applications require digital outputs to switch AC and DC voltage motors on and off and to monitor AC and DC voltages. These AC and high DC voltages cannot be controlled or read directly by the TTL digital lines of a CIO-DIO.

Solid State Relays, such as those available from Computer Boards, Inc. allow control and monitoring of AC and high DC voltages and provide 750V isolation. Solid State Relays (SSRs) are the recommended method of interfacing to AC and high DC signals.

The most convenient way to use solid state relays and a CIO-DIO board is to purchase a Solid State Relay Rack. A SSR Rack is a circuit board with output buffer chips which are powerful enough to switch the SSR and sockets to plug SSRs into. SSR Racks are available from Computer Boards and most manufacturers of SSRs.

The high current outputs of the CIO-DIO24H boards are suitable to drive SSR' directly but the CMOS outputs of the CIO-DIO24 and CIO-DIO24/CTR3 do not have sufficient drive to connect directly to most SSRs. If you only want to drive one or two SSRs with CMOS outputs, all you need is a 74LS244 output buffer chip between the 82C55 output and the SSR. Of course the SSR will need 5 volt power as well.

VOLTAGE DIVIDERS

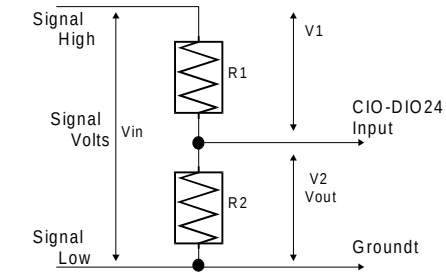
If you wish to measure a signal which varies over a range greater than the input range of a digital input, a voltage divider can drop the voltage of the input signal to the level the digital input can measure.

A voltage divider takes advantage of Ohm's law, which states,

Voltage = Current * Resistance

Implied in the above is that any variation in the voltage drop for the circuit as a whole will have a *proportional* variation in all the voltage drops in the circuit.

A voltage divider takes advantage of the fact that the voltage across one of the resistors in a circuit is proportional to the voltage across the total resistance in the circuit.



The pull-up resistor provides a reference to +5V while its value of 2200 ohms requires only 2.3 mA of drive current

If the 82C55 is reset and enters high impedance input, the line is pulled high. At that point, both the 82C55 AND the device being controlled will sense a high signal.

If the 82C55 is in output mode, the 82C55 has more than enough power (2.5mA) to over ride the pull-up/down resistor's high signal and drive the line to 0 volts. If the 82C55 asserts a high signal, the pull up resistor guaranties that the line goes to +5V.

Of course, a pull-down resistor accomplishes the same task except that the line is pulled low when the 82C55 is reset. The 82C55 has more than enough power to drive the line high.

The CIO-DIO24 series boards are equipped with positions for pull-up/down resistors Single Inline Packages (SIPs). The positions are marked A, B and C and are located beside the 82C55 or output chips.

A 2.2K, 8 resistor SIP is made of 8, 2.2K resistors all connected one side to a single common point and the other, each to a pin protruding from the SIP. The common line to which all resistor are connected also protrudes from the SIP. The common line is marked with a dot and is at one end of the SIP.

The SIP may be installed as pull-up or pull-down. At each location, A, B & C on the CIO-DIO24 series boards, there are 10 holes in a line. One end of the line is +5V, the other end is GND. They are so marked. The 8 holes in the middle are connected to the 8 lines of the port, A, B, or C.

A resistor value of 2.2K is recommended. Use other values only if you have calculated the necessity of doing so.

UNCONNECTED INPUTS FLOAT!

Keep in mind that unconnected inputs float. If you are using the DIO24 board for input, and have unconnected inputs, ignore the data from those lines.

In other words, if you connect bit A0 and not bit A1, do not be surprised if A1 stays low, stays high or tracks A0... It is unconnected and so unspecified. The 82C55 is not malfunctioning. In the absence of a pull-up/down, any input to a CIO-DIO which is unconnected, is unspecified!

You do not have to tie input lines, and unconnected lines will not affect the performance of connected lines. Just make sure that you mask out any unconnected bits in software!

QUICK START

The installation and operation of all three of the CIO-DIO series boards is very similar. Throughout this manual we use CIO-DIO24 as a generic designation for the CIO-DIO24, CIO-DIO24H, CIO-DIO24/CTR3. When required due to the differences in the boards, the specific board name is used.

The CIO-DIO24 boards are easy to use. This quick start procedure will help you quickly and easily setup, install and test your board. We assume you already know how to open the PC and install expansion boards. If you are unfamiliar or uncomfortable with board installation, please refer to your computer's documentation. Though we recommend the use of InstaCal to guide you through your intsallation, detailed written instructions are provided in the next chapter.

> *We recommend you perform the software installation described in sections below prior to installing the board in your computer.* The ***InstaCal***™ operations below will show you how to properly set the switches and jumpers on the board prior to physically installing the board in your computer.

INSTALLING INSTACAL™

Windows (in its various forms) and DOS users install the program by running the INSTALL.EXE program supplied on your InstaCal diskette (future releases of InstaCal will provide SETUP.EXE rather than Install.EXE). It will create all required folders/directories and unpack the various pieces of compressed software. Simply run install/setup and follow the on-screen instructions. Note where the installed files are placed, as you will need to access them in the next step (the default location is on your main hard drive in a directory or folder named C:\CB\).

RUNNING INSTACAL™

To run ***Insta*Cal™** in the various forms of Windows, find the file named InstaCal.exe using your file management system and double click your mouse on it. In DOS simply type *instacal* and press the *Enter* key.

Once running, ***Insta*Cal™** provides four sub-menus (plus exit).

1. Select ***Install*** (either highlight it and hit enter or double click your mouse on it).

2. Select **Board #0** (select another number if Board #0 is already installed)

3. Select **Board Type**

4. Move through the selections and highlight the particular board you are installing (e.g. CIO-DIO24H or CIO-DIO24/CTR3). Either double click on the board or hit enter.

5. The board's default settings are then displayed. The board's defaults are:

BASE ADDRESS:	300H (768 Decimal) Same as data sheet.
WAIT STATE:	OFF.

6. You are now ready to install the board in your computer. Turn off your computer, unplug it from AC power, open your PC and install the board in any unused ISA slot. After the board is installed and the computer is closed up, turn the power back on.

7. Run ***Insta*Cal™** again, and at the main menu select ***Test.***

   a. Select the board you just installed

   b. Select **Internal Test**

   c. The internal control registers of the board will then be tested. If this test is successful, your board is installed correctly. If not, you likely have a base address conflict, or have the base address switch set incorrectly. Please refer to the next chapter for more information regarding selecting and setting the base address.

   d. If the **Internal Test** is completed successfully, you may want to check that the I/O pins are working correctly. To check this select **External Test** and follow the instruction provided. This will require you to use the shorting wires supplied with the board to short inputs to outputs for I/O testing.

ELECTRONICS AND INTERFACING

This short, simple introduction to the electronics most often needed by digital I/O board users covers a few key concepts.

IMPORTANT NOTE

It cannot be stated often enough to those unfamiliar with the 82C55, WHENEVER THE 82C55 IS POWERED ON OR RESET, ALL PINS ARE SET TO HIGH IMPEDENCE INPUT.

The implications of this fact is that if you have output devices such as solid state relays, they may be switched on whenever the computer is powered on or reset. To prevent unwanted switching and to drive all outputs to a known state after power on or reset, pull all pins either high or low through a 2.2K resistor.

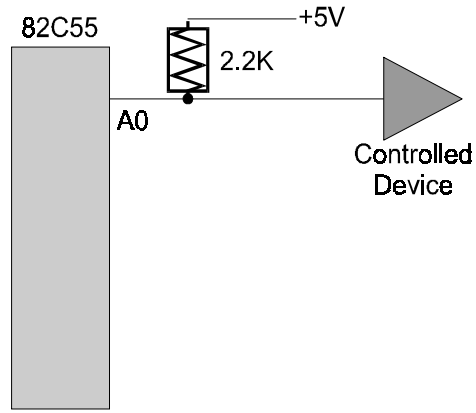
PULL UP & PULL DOWN RESISTORS

Whenever the 82C55 is powered on or reset, the control register is set to a known state. That state is mode 0, all ports input.

When used as and output device to control other TTL input devices, the 82C55 applies a voltage level of 0V for low and 2.5V-5V for high. It is the output voltage level of the 82C55 that the device being controlled responds to.

The concept of output voltage for an 82C55 in input mode is meaningless. Do not connect a volt meter to the floating input of an 82C55. It will show you nothing of meaning. In input mode the 82C55 is in 'high Z' or high impedance. If your 82C55 was connected to another input chip (the device you were controlling), the inputs of that chip are left floating whenever the 82C55 is in input mode.

If the inputs of the device you are controlling are left to float, they may float up or down. Which way they float is dependent on the characteristics of the circuit and the electrical environment; and may be unpredictable! This is why it often appears that the 82C55 has gone 'high' after power up. The result is that you controlled device gets turned on! That is why you need pull up/down resistors.



Shown here is one 82C55 digital output with a pull-up resistor attached.

Output High	2.4V min @ -15mA
Output Low	0.55V max @ 64mA
Input High	2.0V min, 7.0V max
Input Low	0.8V max, -0.5V min

INTERRUPT INPUT

Type	Positive edge triggered.
PC bus IRQ	IRQ2 - IRQ7
Enable	INTERRUPT ENABLE, Pin 2. Enable = LOW Not Enabled = High Tied HIGH through 10K on board.

ENVIRONMENTAL

Operating Temperature	0 - 70 deg C
Storage Temperature	-40 to 100 deg C
Humidity	0 to 90% non-condensing
Weight	5 oz

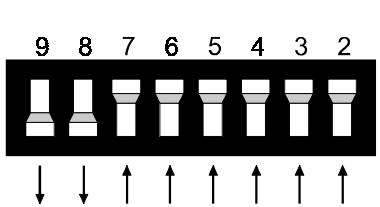
BASE ADDRESS

The simplest way to set the Base address switch is by using InstaCal. This procedure is described in the previous chapter (Quick Start). The following information is provided as a reference and will be useful if you are unable to use InstaCal to guide your installation.

Each I/O board uses one or more I/O address locations within your computer's I/O address space. In order to not interfere with other installed boards, each board must use unique addresses. The BASE ADDRESS determines the board's location within your computer's I/O address space. Most boards will require between 2 and 16 I/O addresses. These are usually consecutive addresses above the BASE ADDRESS (e.g. Base+1, Base+2, ... Base+N).

The BASE ADDRESS switch is the means for setting the base address. Each switch position corresponds to one of the ISA bus address lines. By placing the switch down, the CIO-DIO address decode logic is instructed to respond to that address bit.

A complete address is constructed by calculating the HEX or decimal number which corresponds to all the address bits the CIO-DIO has been instructed to respond to. For example, shown to the right are address 9 and 8 DOWN, all others UP.



BASE ADDRESS SWITCH - Address 300H shown here.

Address 9 = 200H (512D) and address 8 = 100H (256D), when added together they equal 300H (768D).

NOTE!
DO NOT PAY ATTENTION TO THE NUMBERS PRINTED ON THE SWITCH. LOOK AT THE NUMBERS PRINTED IN WHITE ON THE BOARD!

Certain address are used by the PC, others are free and may be used by the CIO-DIO and other expansion boards. We recommend BASE = 300H (768D) be tried first (this is the default address selected on boards as we ship them)

TABLE OF I/O ADDRESSES

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2CF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	82C55 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT) CARD	300-30F	PROTOTYPE
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTYPE CARD
0A0-0A1	8259 PIC#2	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

The CIO-DIO BASE ADDRESS switch may be set for address in the range of 000-3FC and it should not be hard to find a free address area for you CIO-DIO. Once again, if you are not using IBM prototyping cards or some other board which occupies these addresses, then the board's default address of 300 HEX is free to use.

Addresses not specifically listed, such as 390-39F, are not reserved and may be available. Check your computer for other boards which may use I/O addresses.

INTERRUPT LEVEL SELECT

The trigger logic on the CIO-DIO24 is quite simple. Pin 1 of the 37 pin connector is an input jumper which maps the interrupt directly onto the PC bus. The signal to the bus is buffered. The buffer is enabled by a LOW level on Pin 2, interrupt enable.

Most hardware interrupts are assigned by the computer and are reserved for internal system use. However, some are available to you.

SPECIFICATIONS

POWER CONSUMPTION

CIO-DIO24

+5V Supply	170 mA typical / 270 mA max.
+12V Supply	None.
-12V Supply	None.

CIO-DIO24H

+5V Supply	400 mA typical / 625 mA max.
+12V Supply	None.
-12V Supply	None.

CIO-DIO24/CTR3

+5V Supply	190 mA typical / 300 mA max.
+12V Supply	None.
-12V Supply	None.

NOTE

Additional power will be drawn by user's connections to the power pins accessible on CIO-DIO connectors.

DIGITAL I/O

TTL LEVEL DIRECT TO/FROM 82C55 & 82C54 CHIPS

82C55 output high	3.0 V min @ -2.5mA
82C55 output low	0.4 V max @ 2.5 mA
82C55 input high	2.0 V min, 5.5 V max
82C55 input low	-0.5 V min, 0.8 V max
82C55 drive capability	5 LSTTL loads

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	80	128	OUT	OUT	OUT	OUT
0	0	0	1	81	129	OUT	OUT	OUT	IN
0	0	1	0	82	130	OUT	OUT	IN	OUT
0	0	1	1	83	131	OUT	OUT	IN	IN
0	1	0	0	88	136	OUT	IN	OUT	OUT
0	1	0	1	89	137	OUT	IN	OUT	IN
0	1	1	0	8A	138	OUT	IN	IN	OUT
0	1	1	1	8B	139	OUT	IN	IN	IN
1	0	0	0	90	144	IN	OUT	OUT	OUT
1	0	0	1	91	145	IN	OUT	OUT	IN
1	0	1	0	92	146	IN	OUT	IN	OUT
1	0	1	1	93	147	IN	OUT	IN	IN
1	1	0	0	98	152	IN	IN	OUT	OUT
1	1	0	1	99	153	IN	IN	OUT	IN
1	1	1	0	9A	154	IN	IN	IN	OUT
1	1	1	1	9B	155	IN	IN	IN	IN

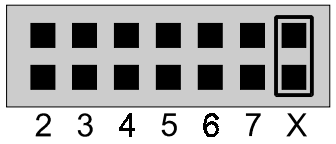
82C54 COUNTER CHIP

The 82C54 counter chip is quite complex. The data sheet for the part contains programming information, input and output timing diagrams and interfacing specifications.

We are sorry, but it is beyond the scope of this manual to reproduce the information, all of which is contained in the chip manufacturers data book. For that information check out Intel's web site at www.intel.com. A variety of information is available and can be found by "searching" on keyword 8254.

NAME	DESCRIPTION	NAME	DESCRIPTION
NMI	PARITY	IRQ8	REAL TIME CLOCK
IRQ0	TIMER	IRQ9	RE-DIRECTED TO IRQ2 (AT)
IRQ1	KEYBOARD	IRQ10	UNASSIGNED
IRQ2	RESERVED (XT) INT 8-15 (AT)	IRQ11	UNASSIGNED
IRQ3	COM OR SDLC	IRQ12	UNASSIGNED
IRQ4	COM OR SDLC	IRQ13	NUMERIC CO-PROC
IRQ5	HARD DISK (AT) LPT (AT)	IRQ14	HARD DISK
IRQ6	FLOPPY DISK	IRQ15	UNASSIGNED
IRQ7	LPT		

There is a jumper block on the CIO-DIO24 located just above the PC bus interface (gold pins). The factory default setting is that no interrupt level is set. The jumper is in the 'X' position.



INTERRUPT JUMPER BLOCK

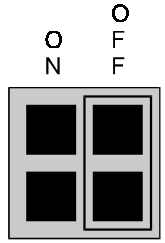
Please leave the jumper in the 'X' position for now. Interrupts are hardware initiated software routines. If the software you are using employs interrupt service routines, it will require you to select an IRQ level.

WAIT STATE JUMPER

The CIO-DIO24 boards have a wait state jumper which can enable an on-board wait state generator. A wait state is an extra delay injected into the processor's clock via the bus. This delay slows down the processor when the processor addresses the CIO-DIO board so that signals from slow devices (chips) will be valid.

The wait state generator on the CIO-DIO is only active when the CIO-DIO is being accessed. Your PC will not be slowed down in general by using the wait state.

Because all PC expansion board busses are slowed to either 8MHz or 10MHz, the wait state will generally not be required.



WAIT STATE JUMPER BLOCK - Place jumper on the two leftmost pins if a wait state is desired. No wait state is selected above.

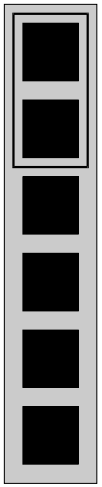
If you experience sporadic errors from the 82C55 digital I/O chip (reset, port direction swaps) you might try enabling the wait state generator.

CIO-DIO24/CTR3 CLOCK JUMPER

The CIO-DIO24/CTR3 has a row of jumpers that allow the XTAL signal to be connected to counter 0 input, and the counters to be chained 0 to1, and 1 to 2.

It is often desirable to chain the output of one counter into the input of another. In this way, a counter of 32 or 48 bits may be constructed from the three 16 bit counter of the 82C54.

Of course the counters may be chained externally through the 37 pin connector, but you may find the jumpers convenient.



XTAL
CTR0

The on-board 10MHz XTAL signal may be connected directly to the Input of Counter 0 by placing a jumper block between the pins marked XTAL and CTR0.

OUT0

The output of counter 0 may be chained directly into the Input of counter 1.

CTR1
OUT1

The output of counter 1 may be chained directly into the input of counter 2.

CTR2

Using the on board jumper block for counter chaining is easier than chaining the counters externally.

CIO-DIO24/CTR3 COUNTER CLOCK SOURCE JUMPER

For information on modes 1 (strobed I/O) and 2 (bi-directional strobed I/O), you will need to acquire an Intel or AMD data book and see the 82C55 data sheet.

7	6	5	4	3	2	1	0
MS	M3	M2	A	CU	M1	B	CL
	Group A				Group B		

The 82C55 may be programmed to operate in Input/ Output (mode 0), Strobed Input/ Output (mode 1) or Bi-Directional Bus (mode 2).

NOTE!
Only 82C55 mode 0 is avalable on the CIO-DIO24H.

Included here is information on programming the 82C55 in mode 0. Those wishing to use the 82C55 in modes 1 or 2, or who wish to program the 82C54 counter on the CIO-DIO24/CTR3, must procure a data book from Intel Corporation Literature Department.

When the PC is powered up or RESET, the 82C55 is reset. This places all 24 lines in Input mode and no further programming is needed to use the 24 lines as TTL inputs.

To program the 82C55 for other modes, the following control code byte must be assembled into an 8 bit byte.

MS = Mode Set. 1 = mode set active

M3	M2	Group A Function	
0	0	Mode 0	Input/Output
0	1	Mode 1	Strobed Input/Output
1	X	Mode 2	Bi-Directional Bus

A	B	CL	CH	Independent Function
1	1	1	1	Input
0	0	0	0	Output

M1 = 0 is mode 0 for group B. Input / Output
M1 = 1 is mode 1 for group B. Strobed Input / Output

The Ports A, B, C High and C Low may be independently programmed for input or output.

The two groups of ports, group A and group B, may be independently programmed in one of several modes. The most commonly used mode is mode 0, input / output mode. The codes for programming the 82C55 in this mode are shown below. D7 is always 1 and D6, D5 & D2 are always 0.

Base Address +0

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0
Pin 30	Pin 31	Pin 32	Pin 33	Pin 34	Pin 35	Pin 36	Pin 37

Port B Data
Base Address +1

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10

Ports A & B may be programmed as input or output. Each is written to and read from in Bytes, although for control and monitoring purposes the individual bits are more interesting.

Bit set/reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

Port C Data
Base Address +2

7	6	5	4	3	2	1	0
C8	C7	C6	C5	C4	C3	C2	C1
CH4	CH3	CH2	CH1	CL4	CL3	CL2	CL1
Pin 22	Pin 23	Pin 24	Pin 25	Pin 26	Pin 27	Pin 28	Pin 29

Port C may be used as one 8 bit port of either input or output, or it may be split into two 4 bit ports which may be independently input or output. The notation for the upper 4 bit port is PCH3 - PCH0, and for the lower, PCL3 - PCL0.

Although it may be split, every read and write to port C carries 8 bits of data so unwanted information must be ANDed out of reads, and writes must be ORed with the current status of the other port.

OUTPUT PORTS

In 82C55 mode 0 configuration, ports configured for output hold the output data written to them. This output byte may be read back by reading a port configured for output.

INPUT PORTS

In 82C55 mode 0 configuration, ports configured for input read the state of the input lines at the moment the read is executed, transitions are not latched.

I/O CONNECTIONS

CABLES AND SCREW TERMINAL BOARDS

The CIO-DIO24 connector is accessible through the computer's expansion bracket. The connector is a standard 37 pin male connector. The I/O connections can be brought out to easy to use screw terminals by purchasing a CFF37-series cable and a CIO-MINI-37 screw terminal accessory board.

A mating female connector may be purchased from Radio Shack and most other electronic supply outlets.

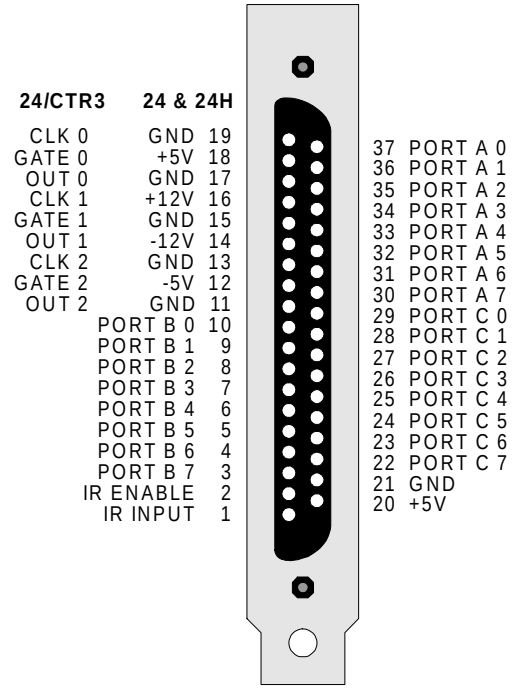
CONNECTOR DIAGRAM - CIO-DIO-24, -24H & -24/CTR3

The CIO-DIO24 I/O connector is a 37 pin D type connector accessible from the rear of the PC through the expansion backplate. The signals available are direct connections to an 82C55 digital I/O chip as well as the PC's internal power supplies. The pin-out is identical to the MetraByte PIO-12.

The CIO-DIO24/CTR3 adds the signals for an 82C55 counter chip in place of the PC power connections..

The connector accepts female 37 D type connectors, such as those on the C37FF-2, 2 foot cable.

If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-MINI37 or CIO-SPADE50 screw terminal boards.



SIGNAL CONNECTION CONSIDERATIONS

All the digital outputs and inputs on the CIO-DIO24 and CIO-DIO24/CTR3 connector are CMOS TTL. The CIO-DIO24H signals are buffered (high output drive) TTL. TTL is an electronics industry term, short for Transistor Transistor Logic, which describes a standard for digital signals which are either at 0V or 5V.

The voltages and currents associated with external devices range from less than a hundred mA at a few volts for a small flash light bulb to 50 Amps at 220 volts for a large electric range. Attempting to connect either of these devices directly to the CIO-DIO could damage the I/O chip.

In addition to voltage and load matching, digital signal sources often need to be debounced. A complete discussion of digital interfacing will be found in the section on Interface Electronics in this manual.

IMPORTANT NOTE

The 82C55 digital I/O chip initializes all ports as inputs on power up and reset. A TTL input is a high impedence input. If you connect another TTL input device to the 82C55 it will probably be turned ON every time the 82C55 is reset, or, it might be turned OFF instead. Remember, the 82C55 which is reset is in INPUT mode.

To safegaurd against unwanted signal levels, all devices being controlled by an 82C55 should be tied low (or high, as required) by a 2.2K ohm resistor.

You will find positions for pull up and pull down resistor packs on your CIO-DIO24 series board. To implement these, please turn to the application note on pull up/down resistors.

82C55 CONTROL & DATA REGISTERS

Each CIO-DIO24 is composed of 82C55 parallel I/O chips (or a TTL implementation of 8255 mode 0). Each board uses 3 data and one control register and occupies 4 consecutive I/O locations. The CIO-DIO24/CTR3 uses 4 additional I/O registers to read and write to the 82C54.

The CIO-DIO24 series boards are easy to program with direct I/O register reads and writes. A tutorial describing how to go about register I/O is beyond the scope of this manual. However, it will be covered in most Introduction To Programming books, available from a bookstore.

As alternatives to register level programming, the CIO-DIO24 series of boards is fully supported by the optional Universal Library software as well as most high level data acquisition and control application packages (e.g. HP Vee or Labtech Notebook).

The registers and their function are summarized in the following table. A more detailed description of each register is included in subsequent sections. Within each register are 8 bits which may constitute a byte of data or 8 individual bit set/read functions.

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE +0	Port A Input of 82C55 #1	Port A Output
BASE +1	Port B Input	Port B Output
BASE +2	Port C input	Port C Ouput
BASE +3	None. No read back on 82C55.	Configure 82C55 #1
	CIO-DIO24/CTR3 ADDTIONAL REGISTERS	
BASE +4	Counter 0	Counter 0 Load
BASE +5	Counter 1	Counter 1 Load
BASE +6	Counter 2	Counter 2 Load
BASE +7	None	Counter Control

82C55 DIGITAL I/O REGISTERS

Port A Data